Mahita Nagabhiru

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Research Interests:

- Computer Architecture
  - Scalable cache coherence and synchronization models, NVMs, Transactional Memories
  - Distributed systems architecture
  - SIMD architecture – GPGPUs and vector processors
  - Advanced micro-architecture - superscalar microarchitecture, complexity-effective processors, multithreading, advanced speculation techniques, fault-tolerant microarchitectures
- Digital VLSI Design
  - Timing-aware and power-aware RTL design and synthesis
  - Automate development and verification of entire design's timing constraints from RTL to PD timing closure

Educational Qualifications:

- **PhD in Computer Engineering** — Aug-2021 (expected)
  North Carolina State University, USA — GPA: 3.67/4.0
- **B.E (Hons) Electronics and Instrumentation** — May-2011
  Birla Institute of Technology and Science, Pilani, India — GPA: 8.23/10.0
- **Intermediate (Std XII):** — May-2007
  Board of Intermediate Examination, A.P — Percentage: 96.1%
  - Stood in **the top 1%** in the state of Andhra Pradesh, India
- **High School (Std X):** — May-2005
  Central Board of Secondary Education — Percentage: 97.6%
  - 3rd rank at **All India** Level in CBSE board of education and **Valedictorian** for my school.

Publications and Presentations:

- Placement Aware Clock Gate Cloning and Redistribution Methodology, International Symposium on Quality Electronic Design 2012, TIITC 2011
- Clock Tree Considerations for Improved Quality and Robustness, Magma Users Summit on Integrated Circuits 2011
- Clock Tree Synthesis Care-about for Complex SoCs, Design Automation Conference 2012

US Patent:

- Placement aware clock gate cloning and fan-out optimization- number: **8,661,374**

Awards/Honours:

- Recipient of Fellowship of merit from NCSU graduate school in academic year 2015-16.
- Recipient of merit-cum-need **scholarship** of BITS, Pilani –Goa campus.
- Recipient of PM scholarship for deserving Ex-servicemen wards for pursuing undergraduate studies.

- Stood in top 1% during intermediate in the State of Andhra Pradesh (11^{th}-12^{th} Std).
- Secured **all India 3rd Rank** in Kendriya Vidyalaya Sangathan for matriculation and stood as **Valedictorian** for my school; Had received a scholarship for the same from CBSE board. (10^{th} Std)

Extra-curricular Activities:

- Member of **Women in Engineering** group at NCSU and was graduate student representative in Evaluation of Teaching Committee for the year 2016-2017.
- Member of **ACM** SigARCH and WIARCH. Attended CRA-W 2018 grad cohort workshop.
- Member of **Student Council Affairs** as treasurer at BIT Pilani, Goa for the year 2009-2010.
- Was member of **Abhigyan (teaching program for kids)** for two years at BITS-Pilani Goa campus.
- Participated and organized workshops by EE department during Quark 2008 and 2009- technical festival at BITS Pilani, Goa.
- First prize for meritorious performance for "17^{th} **National Youth Parliament Competition**" by Ministry of Parliamentary Affairs, India at Regional level 2004-05. This is an event where students assemble in mock parliament sessions to discuss the contemporary problems faced by the nation and providing possible solutions to resolve it as a Politician.
- Multiple prizes at school and regional levels for various cultural events throughout school
    - Third in **Sanskrit recitation** competition in 2002-03.
    - First prize in 2000 for Group Song and Dance performance during Social Science Exhibition cum Cultural Competition 2000, K.V. No.2 AFS, Tezpur, Assam.
    - First in solo dance competition at school level for **Kuchipudi performance** 1999 and 2000, K.V. (AFS) Jorhat, Assam.
    - Special mention and cover by regional Doordarshan TV program for Dance performance for School Annual day 1999, Jorhat Assam.

Graduate Coursework

Computer Design and Technology, Architecture of Parallel Computers, Code Generation and Optimization, Digital ASIC Design, Advanced Microarchitecture, Advanced Parallel Computer Architecture, Operating Systems Principles, GPU Architecture (GPGPUs), Computer Networks, Embedded Systems, Behavioural Synthesis using ROSE compiler (Independent Study)

Graduate Projects

Computer Architecture:

- Currently working on modelling *TLE (transactional lock elision)* on GEM5 simulator. This has multiple aspects to it- designing the right workload model, modifying the pipeline and instruction set to understand transactional commands and finally changing coherence protocol to understand transactional semantics in SLICC.
- Implemented *Victim Replication* on GEM5. Here I used the SLICC files to create the Victim Replication Protocol and analyzed the results for PARSEC benchmarks.
- Designed a cycle-accurate simulator for *Dynamic Instruction Scheduling in out-of-order Superscalar Processor* using C++; features included multi-functional execution units, configurable scheduler and superscalar widths. Further, Simulated *Trace processor* micro-architecture with *Control Independence* optimization unit on a detailed C++ superscalar functional simulator.
- Designed a Simulator for a *Multilevel Cache* in C++ with *WBWA, WTNA write policies* and *LRU replacement policy*. Used the generic Cache module to have Victim cache for L1 Cache. Further

enhanced this Cache module to implement *bus based Cache Coherence Protocols (MSI, MESI, MOESI, Dragon*) in a Symmetric Multiprocessor (SMP)-like environment with *L2 as shared cache*.

- Simulated a configurable *branch predictor* with BTB for *Bimodal, Gshare and Hybrid* predictors and analyzed for various configurations.

Compiler Optimizations (used LLVM IR):

- Implemented *an LLVM bitcode generator* for a subset of the C language using LLVM C APIs. Also, implemented libraries to perform Common *Sub-Expression Elimination* (CSE), *Dead Code Elimination* (DCE), *Loop Invariant Code Motion* (LICM) optimization passes, to gather vital statistics of an LLVM module and to identify *SIMD Vectorization* opportunities in LLVM IR.

Digital ASIC Design:

- Designed and Simulated *a hardware accelerator for Bellman Ford Algorithm* to workout shortest spanning tree between two nodes in a network using Verilog HDL. Synthesized the design with timing constraints and optimized the design for performance with product of area, clock frequency and execution time as metric.

Academic Experience (Graduate)

- **Teaching Assistant, North Carolina State University (Aug-2015 to present, 2.5years)**
  With Department of Electrical and Computer Engineering

  Areas of work*:* Working as a Teaching Assistant for various courses like Introduction to Computer Systems (undergraduate course), Computer Design and Technology, Architecture of Parallel Computers (graduate course) and Compiler design & Optimization. As a part of this, I am responsible for *taking tutorial classes* **and holding additional tutorial hours** for the course. Also, I am critical in the *evaluation* of all the course components, maintaining *courses' websites* and Q&A forums.

- **Independent Study, North Carolina State University (Jan-2016 to May-2016, 6mons)**
  With Prof. Eric Rotenberg
  Work: Worked on enhancing an in-house compiler (based on ROSE) to target Behavioural synthesis. Intent was to convert any C/C++ based Hardware simulators seamlessly into synthesizable Verilog RTL.

Professional Experience:

(see page 4 for further description)

- **Graphene Semiconductor Services Pvt Ltd (Apr-2014 to May-2015)**
  Member Technical Staff
  Areas of work: On-site customer support to crucial customers like Sandisk and Lantiq communications as a Static Timing Analysis expert. Activities involve driving timing closure of the chips, complete constraints development and verifications and provide CTS strategies for PnR team.

- **Texas Instruments (June-2011 to Apr-2014, 2yrs 11mons)**
  Design Engineer

Areas of work: Worked on 28nm and 40nm technology nodes in various Physical Design and Static Timing Analysis roles. Ownership of the design library for entire SoC team, PnR experiments for various Sub-blocks, Netlist to GDSII flow flush of a crucial test-chip and development of timing constraints for various block/top level of the SoCs.

Academic Experience (undergraduate):

- **Analog Electronics, BITS-Pilani, Goa Campus (Jan-May2011, 6mons)**
  With Asst. Prof. Ramesha C. K
  Areas of work*:* Worked a Professional Assistant for the course Analog electronics on campus. As a part of this, was responsible for **assisting in the lab sessions** for the course. Coordinated the question paper making and evaluation for the simulation lab component (using circuit design in PSPICE) for the course.

Undergraduate Projects:

- Design of a Placement Aware clock gate cloning and optimization Algorithm.
- Achieving Very Low Clock Tree Skews with Clock Meshes.
- Design of a smart water tank using Intel 8086 microprocessor.
- Design of 4-bit ripple carry adder.
- Comparison of different suppression and attenuating filters in MATLAB to sharpen an image.
- Synthesis, Implementation and Analysis of various Pass Transistor Logic Circuits and Current Mirror Circuits.

Undergraduate Coursework:

Analog & Digital VLSI Design, Microelectronic Circuits, Digital Electronics & Computer Organization, Microprocessor Programming & Interfacing, Electronic Devices & Integrated Circuits, Analog Electronics, Circuits and Signals, Control Systems, Electrical Sciences I & II, Data Communications & Networking, Communication Systems, Power Electronics, Transducers, Industrial Instrumentation Control, Electronic Instruments and Instrumentation Technology, Image Processing

Skill Set:

- **Computer Languages:** C++, Verilog, Assembly level programming of x86, SPICE, Perl, Tcl.
- **CAD Tools:** Cadence RC Compiler, Synopsys DC compiler, Cadence Encounter Timing System, Talus, Synopsys ICC, Synopsys PrimeTime, Cadence Virtuoso Schematic & Layout Editor, Microwind, ModelSim-Se.
- **Software Packages:** MATLAB, Simulink, AutoCAD, NI LabVIEW, PLC
- **Operating Systems:** Windows, Linux.

Work Experience (Detailed):

- **Graphene Semiconductor Services Pvt Ltd (Apr-2014 to May-2015)**
  Member Technical Staff, STA
  - **28nm SoCs at Qualcomm, Bangalore**
    - Was part of CAD team that handled entire STA flow for varies subchips part of the SoCs at 28nm technology node and provided seamless flow for Timing analysis, provide CTS strategies and setup/hold fixes for all the blocks.

- **28nm SoC (Primarily intended for DSL applications) at Lantiq Communications India Pvt. Ltd.**
  - Owner for the top-level Netlist synthesis delivery. This involves verification and modeling of appropriate timing constraints for synthesis and constant support for the PD team apart from making sure the synthesized Netlist is complete wrt all Quality Checks. This SoC had critical IO interfaces like **Media Independent Interface (GMII/RGMII), Serial Communication Interface (SCI) and Management Engine Interface (Intel and Motorola MEI).**
- **28nm SoC (USB 3.0 controller IP) at Sandisk, Bangalore.**
  - Provided complete support in the timing closure for the entire SoC in fuctional mode. The design was very complex and had huge congestion issue and the trick was in fixing timing using useful clock skew and minimizing the buffer insertion in turn saving on area and congestion.

- **Texas Instruments, Bangalore (June-2011 to Apr-2014, 2yrs 11mons)**
  Design Engineer in PD/STA.
  - **28nm SoC: (May-2014 tape-out)**
    Worked on a TI-DSP-c66x based SoC customized for automotive market specifically automatic driver assistance system. As a part of the PD team here,
    - **Complete ownership of shift** mode timing constraints and closure for top-level. Driving constant interaction and feedback with the DFT team for right TESOC implementation to avoid unexpected hiccups late in the design apart from constraints development and flow flush for STA.
    - Responsible for the driving and monitoring of **the entire constraints QC flow** including top-level as well as all the subchips. This includes key focus on generated clocks' waveform verification, re-convergence points' identification and getting exceptions in place right from synthesis onwards to have smooth timing closure.
  - **45nm SoC: (tape-out done in Aug-2013)**
    This was a cortex-A9 based **power-optimized** application processor, intended for POS and industrial markets with differentiating **security** features. This design with ~50mm2 die size had multiple differentiating IPs that were successfully accommodated very late in the design without losing sight of the goals set in the beginning be it power, performance or the re-usability. Played the following roles as part of this team:
    - Had **complete ownership of the design library**. This included library maintenance, QC of the whole library and block level QC, volcano creation & QC and timely feedback to the various IP teams.
      Efficiently tracked the multiple & untimely releases of various IPs, provided **constant feedback** to the various IP teams for the right data, dealt with toolkit support for **QC process** to get things done on time, had every flow/data **documented & versioned** apart from hacking the flow/ data to enable seamless working of the design team when needed. This experience also gave a **wholesome picture** of the minutest data needed for a design to be complete.

- **Complete ownership of constraints development and verification** of 7/10 subchips present in the design. These blocks included the logic involved for **USB**, **Ethernet**, **tamper-proofing** support and **industrial communication control.**
  Because of quick learning nature and love for clarity of problem at hand, acquired knowledge on the functionality of various blocks, completely **traced right clock structures** using timing tools and was able to successfully provide constraints for multiple blocks with varied complexities-few imposing challenges with **multiple clock domain interaction**, few with **source synchronous** clocking while others with complicated **cascaded clock** structures.
  Also played key role in enhancing constraints generation flow and co-owned setting in place the constraints verification flow for the whole design.

- Also **owned/co-owned the timing closure** for the subchips mentioned above apart from providing CTS strategies. The blocks that were especially tricky were related to **general purpose IO control, advanced encryption support and interconnect network for the SoC.**
  With clear understand of the clock structures, provided **CTS strategy** for the blocks and fully owned timing closure for a couple of blocks and helped with critical paths on the others. As a part of this, **completely owned QC for the STA setup** for the subchips timing closure, and **created** the **hold-fixing flow/guideline** used across the design.

- **Owned SDF generation and handoff flow for the full project**. This included constant interaction with the verification and DFT teams for the various inputs needed and fully responsible for setting up and QC of the SDF generation flow and making timely handoffs.

- During the trail flow flush, contributed to getting confidence on DAE area estimates, architecture being planned and power estimation for 2 of the blocks used in the design. These blocks had new and innovative RTL and were **very crucial for the SoC**. These had the differentiating security features intended for **tamper-proofing and on-the-fly encryption.** Performed **various floor-plan trials** to see if the timing, area and power targets can be met with the new RTL.

- **Test-chip: (tape-out done in march-2012)**
  - As a part of the 45nm SoC, a critical **one-of-a-kind frequency and voltage monitoring** circuit was to be introduced which had to be tested on silicon before taking into the actual chip. This was also very critical from a power point of view and had a custom memory designed for its sole implementation.

  Completely owned the entire setup process for this test-chip from netlist to layout to get a first-hand experience of **the entire synthesis to gdsii flow** and streamlined the whole flow from synthesis to backend checks.

Undergraduate Internship (detailed):

- **Texas Instruments India, Bangalore (July-Dec 2010, 6mons)**
  - **Design of a Placement Aware Clock Gate Cloning and Optimization Algorithm**
    - Designed an algorithm to optimize placement and cloning of clock gates based on proximity to its sinks to achieve low skew for minimal resources.
      This is a flow that very **efficiently saves on power and area** by cutting down the number of CT-elements used, minimizing clock tree divergence and clock net and achieving **optimal local skew**.
      This is actively getting used in TI for multiple SoCs/subchips. E.g.: top-level logic for the 45nm SoC mentioned above and its core processor sub-system, the core processor sub-system inside Sitara-AM335x etc- these modules were both **performance and power critical**.
  - **Achieving Very Low Clock Tree Skews with Clock Meshes.**
    - Completed a quantitative study to achieve very low clock skew for high speed designs using clock mesh structures. This was mainly intended for implementation on **processor sub-systems** which are highly **performance critical**.